CLMPTO

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CLAIMS 1 – 37 (CANCELLED)

38. (Original) An array substrate for X-ray detector, comprising:

a substrate having a switching region and a pixel region;

a gate line on a substrate, the gate line having a gate pad at the end thereof;

a gate insulation layer on said gate line;

a data line on said gate insulation layer, the data line perpendicularly crossing said gate line to define the pixel region and contacting a data pad at the end thereof;

a thin film transistor in the switching region near the crossing of the said gate and data lines, the thin film transistor including a gate electrode, an active layer, a source electrode, a drain electrode and said gate insulation layer;

a ground line crossing said pixel region parallel with the data line and contacting a ground pad at the end thereof;

a first passivation layer covering said thin film transistor and having a drain contact hole that exposes the drain electrode and a ground line contact hole that exposes the ground line;

a second passivation layer on the first passivation layer, the second passivation layer having a second drain contact hole that exposes the drain electrode and a second ground line contact hole that exposes the ground line;

a first capacitor electrode on the second passivation layer, the first capacitor electrode contacting the ground line through said contact holes that expose the ground line;

an auxiliary drain electrode on the second passivation layer, the auxiliary drain electrode contacting the drain electrode through said first and second drain contact holes;

a third passivation layer on the second passivation layer, the third passivation layer covering the auxiliary drain electrode and the first capacitor electrode, and having an auxiliary drain contact hole that exposes said auxiliary drain electrode; and

a second capacitor electrode on the third passivation layer, the second capacitor electrode electrically contacting the drain electrode and overlapping the first capacitor electrode thereby forming a storage capacitor with the first capacitor electrode and the third passivation layer.

39. (Original) A method of fabricating an array substrate for X-ray detector, comprising:

forming a gate line on a substrate that has a switching region and a pixel region, the gate line having a gate pad at the end thereof;

forming a gate insulation layer on said substrate to cover said gate line;

forming a data line on said gate insulation layer, the data line perpendicularly crossing said gate line to define the pixel region and contacting a data pad at the end thereof;

forming a thin film transistor in the switching region near the crossing of the said gate and data lines, wherein the thin film transistor includes a gate electrode, an active layer, a source electrode, a drain electrode and said gate insulation layer;

forming a ground line that crosses said pixel region parallel with the data line and contacts a ground pad at the end thereof;

forming a first passivation layer covering said thin film transistor and having a first drain contact hole that expose the drain electrode and a first ground line contact hole that exposes the ground line;

forming a second passivation layer on the first passivation layer, the second passivation layer having a second drain contact hole that exposes the drain electrode and a second ground line contact hole that exposes the ground line;

forming a first capacitor electrode on the second passivation layer, the first capacitor electrode contacting the ground line through said first and second ground line contact holes;

forming an auxiliary drain electrode on the second passivation layer, the auxiliary drain electrode contacting the drain electrode through said first and second drain contact holes;

forming a third passivation layer on the second passivation layer, the third passivation layer covering the auxiliary drain electrode and the first capacitor electrode, and having an auxiliary drain contact hole that exposes said auxiliary drain electrode; and

forming a second capacitor electrode on the third passivation layer, the second capacitor electrode electrically contacting the drain electrode and overlapping the first capacitor electrode thereby forming a storage capacitor with the first capacitor electrode and the third passivation layer.

CLAIMS 40 – 74 (CANCELLED)